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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARK FLOOD, MARK RUETTY,
and ANTHONY CACHAT

Appeal 2009-006033
Application 09/862,941
Technology Center 2400

Decided: October 28, 2009

Before KENNETH W. HAIRSTON, KARL D. EASTHOM, and THOMAS S. HAHN, *Administrative Patent Judges*.

HAHN, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants invoke our review under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1 and 3-53. We have jurisdiction under 35 U.S.C. § 6(b). We reverse.

STATEMENT OF THE CASE

Appellants claim a control system invention that has a time synchronization apparatus for synchronizing operation between first and second controllers. The time synchronization apparatus is configurable to operate as both a synchronization master or a synchronization slave.[1] Claim 1, with disputed limitation emphasized, is illustrative:

> 1. A time synchronization apparatus for synchronizing operation of a first controller with that of a second controller in a control system, the synchronization apparatus comprising:
>
> a processor interface for interfacing the synchronization apparatus with a host processor, *the time synchronization apparatus is configurable to operate as both a synchronization master and a synchronization slave*;
>
> a transmitter adapted to transmit synchronization information and data to a network in the control system;
>
> a receiver adapted to receive synchronization information and data from the network; and
>
> a timing system with a clock that maintains an indication of time according to information received from one of the network and the host processor.

The Examiner relies on the following prior art references to show unpatentability:[2]

Yamanaka	US 4,807,259	Feb. 21, 1989

[1] *See generally* Spec., 4:26-29, 9:18-26, 10:10-31, 38:24-29; Figs. 1, 2, 33, and 34.

[2] Filing dates for these documents precede Appellants' earliest effective filing date and are not at issue.

Voth	US 6,199,169 B1	Mar. 6, 2001
Ramussen	US 6,449,732 B1	Sep. 10, 2002
Kuribayashi	US 6,775,246 B1	Aug. 10, 2004

Rejections[3]

1. The Examiner rejected claims 1, 3-7, 13-28, 30-34, 38-46, and 48-53 under 35 U.S.C. § 103(a) as unpatentable over Yamanaka and Voth (Ans. 5-25).
2. The Examiner rejected claims 8-12 under 35 U.S.C. § 103(a) as unpatentable over Yamanaka, Voth, and Rasmussen (Ans. 25-28).
3. The Examiner rejected claims 29, 35-37, and 47 under 35 U.S.C. § 103(a) as unpatentable over Yamanaka, Voth, and Kuribayashi (Ans. 28-31).

Rather than repeat the arguments of Appellants or of the Examiner, we refer to the Briefs and the Answer[4] for their respective details. In this decision, we have considered only those arguments actually made by

[3] Claim 1 is reported in the Examiner's Answer as rejected under 35 U.S.C. § 112, 1st ¶ (Ans. 3, 4). Based on the record, we presume this rejection, which is repeated from the Final Action, mailed Dec. 27, 2007, is an error. The Advisory Action, mailed Mar. 19, 2008, reports that the identical § 112 rejection is "withdrawn because of persuasive argument" in Appellants' Feb. 27, 2008 filed Reply to Final Office Action. The Examiner's Answer neither acknowledges nor distinguishes from the prior withdrawal of this § 112 rejection, and, therefore, there is no ground(s) of record for reasserting the rejection.

[4] We refer throughout this opinion to (1) the Appeal Brief filed May 27, 2005, (2) the Answer mailed Aug. 6, 2008, and (3) the Reply Brief filed Oct. 6, 2008.

Appellants. Arguments that Appellants could have made but did not make in their Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Appellants' Arguments

Appellants collectively argue rejected claims 1, 3-7, 13-28, 30-34, 38-46, and 48-53, which include all appealed independent claims, by asserting *inter alia* that neither Yamanaka nor Voth, alone or in combination, discloses every independent claim recited limitation (App. Br. 6-8). Specifically, Appellants assert that Yamanaka fails to disclose an independent claim 1 limitation for a "'time synchronization apparatus [] *configurable to operate as both a synchronization master and a synchronization slave*'" (App. Br. 7). Further, Appellants assert that "independent claim 38 (and similarly [independent] claims 39 and 52) recites, 'a synchronization circuit . . . *configurable by the host* [processor]'" (*id.*), and that Yamanaka fails to disclose this subject matter.

Appellants address rejected dependent claims 8-12 by referring back to the arguments directed to Yamanaka and Voth as failing to teach or suggest the base independent claim 1 disputed limitation, and assert that Rasmussen alone or in combination does not cure the deficiency (App. Br. 12, 13).

Then for rejected dependent claims 29, 35-37, and 47, Appellants again refer back to the arguments directed to Yamanaka and Voth as failing to teach or suggest the base independent claim 1 disputed limitation for grouped claims 29 and 35-37, or failing to teach or suggest the equivalent limitation from independent claim 39 for dependent claim 47. Referencing

these arguments, Appellants assert that Kuribayashi alone or in combination with Yamanaka and/or Voth does not cure the deficiency (App. Br. 13).

ISSUES

1. Under § 103(a), have Appellants shown the Examiner erred in rejecting claim 1 by finding that Yamanaka and Voth, either alone or in combination, teaches or suggests a time synchronization apparatus "configurable to operate as both a synchronization master and a synchronization slave?"
2. Under § 103(a), have Appellants shown that the Examiner erred in rejecting claims 8-12 by finding that Yamanaka, Voth, and Rasmussen, either alone or in combination, teaches or suggests a control system having an apparatus configurable to operate as "both a synchronization master and a synchronization slave?"
3. Under § 103(a), have Appellants shown that the Examiner erred in rejecting claims 29, 35-37, and 47 by finding that Yamanaka, Voth, and Kuribayashi, either alone or in combination, teaches or suggests a control system having an apparatus configurable to operate as "both a synchronization master and a synchronization slave?"

FINDINGS OF FACT

The record supports the following Findings of Fact (FF) by a preponderance of the evidence:

Appellants' Disclosure

1. According to Appellants' Specification, "control events can be coordinated according to a master synchronization time value," and "synchronization components . . . can be configured as master or slave, wherein slaves within a time zone receive synchronization information from a local master, and wherein a system master provides synchronization information to local masters in other time zones." Spec. 4:20-29.

Yamanaka

2. Yamanaka discloses a time synchronization apparatus and method for use with multiple station systems used to control and send commands to electrical power protection apparatuses. The Yamanaka disclosed time synchronization apparatus includes a master clock at a master station with slave clocks at the slave stations. Yamanaka, col. 1, ll. 15-22; col. 2, ll. 29-37; col. 5, ll. 5-18; Figs. 3A and 3B.

Voth

3. Voth discloses "a system and method for synchronizing the real time clocks within the nodes of a computer cluster." Voth, col. 1, ll. 14-17.
4. The Voth computer cluster is disclosed as a series of interconnected nodes 102a-d, each having a processor 202, memory 204, and time clock 212; and as further disclosed one of the nodes "assumes master role [and] [t]he remaining nodes 102 function as slaves . . ." to ensure each slave clock 212 is synchronized. Voth, col. 4, ll. 17-42; col. 10, ll. 44, 45, and 53-55; col. 13, ll. 61, 62; col. 14, ll. 9, 10; Figs. 1 and 2.

Rasmussen

5. Rasmussen discloses a computerized control system and method using synchronized multiple processor control units for gathering sensor data. Rasmussen, col. 1, ll. 15-21.

Kuribayashi

6. Kuribayashi discloses a communication control apparatus and method for a network, such as a local area network (LAN), that sets synchronization for a master and slaves through referencing stored information. Kuribayashi, col. 1, ll. 7-17.

PRINCIPLES OF LAW

"[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). It is incumbent upon the Examiner, if rejecting claims under 35 U.S.C. § 103, to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073-74 (Fed. Cir. 1988). The factual determinations are set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966) (stating that 35 U.S.C. § 103 leads to required factual inquiries: the scope and content of the prior art, the differences between the prior art and the claims at issue, and the level of ordinary skill in the art). Furthermore,

> "there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" . . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of

> the inferences and creative steps that a person of ordinary skill in the art would employ.

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 418 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

ANALYSIS

Obviousness over Yamanaka and Voth

Claims 1, 3-7, 13-28, 30-34, 38-46, and 48-53

Appellants collectively argue these claims (App. Br. 6-11), and acknowledge that independent claims 38, 39, and 52 recite similar limitations to an independent claim 1 disputed limitation that is argued (App. Br. 7). The claim 1 disputed limitation is a time "synchronization apparatus [] configurable to operate as both a synchronization master and a synchronization slave." Accordingly, we select claim 1 as representative. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Based on the record, we are persuaded the Examiner erred in rejecting claim 1.

The Examiner's reasoning and rationale for finding Yamanaka teaching or suggesting the disputed limitation is: "see Yamanaka Figure 3A; Figure 3B; col. 1, lines 15-22; col. 2, lines 29-37; Figure 3A; col. 5, lines 5-9: configurable to operate as a master; Figure 3B; col. 5, lines 12-18: configurable to operate as a slave" (Ans. 5, 17, 18, and 24). Appellants contest these findings by asserting that "Yamanaka discloses synchronizing a slave clock, [but] . . . is silent as to whether these stations are configurable" (App. Br. 7). Additionally, Appellants argue that "the prior art only teaches a single configurable state while applicants' specification (and the claimed

subject matter) clearly recites that the apparatus can be configurable as both" (Reply Br. 3).

From Appellants' Specification we find disclosures that "synchronization components . . . can be configured as master *or* slave" (FF 1) (emphasis added), which we conclude conforms recited subject matter to Specification disclosures and thereby accords with 37 C.F.R. §1.75(d)(1). We further find Yamanaka teaching a multiple station system with a master station that includes a master clock, and slave stations with slave clocks (FF 2). However, we are unable to reasonably ascertain that Yamanaka teaches or suggests using a processor or some other circuit to arrange the station equipment to operate as masters or slaves for transmitting and receiving synchronization information.

The Examiner in the "Response to Argument" section of the Examiner's Answer indicates further findings concerning configurability that are premised from Voth.

> Yamanaka clearly discloses the existence of master clocks and slave clocks. *Yamanaka does not discourage the configurability of a host system as a slave or a master*, therefore does not teach away from this feature within Voth. Voth discloses that one of the time synchronization nodes assumes a master role which is equivalent to one of the nodes being configured as a master. One network node is a master node and the other nodes are slave nodes. The claim limitation discloses the designation or configuration of a clock as a master and the designation or configuration of a clock as a slave. Yamanaka and Voth reject [sic] the master/slave configuration limitation.

(Ans. 36) (emphasis added).

Later in the "Response to Argument" section, the Examiner indicates that Voth "discloses that one node assumes master status (see Voth col. 4,

lines 35-42: master node) and is configured to perform the master node time synchronization type functions. (see Voth col. 10, lines 44-45; col. 10, lines 53-55; col. 13, lines 61-62; col. 14, lines 9-10: configuration of master node)" (Ans. 37). We also find Voth teaching that a node can "assume" master status (FF 4). Appellants argue that Voth "does not expressly disclose that nodes are configurable . . . ." (App. Br. 8). Appellants' earlier referenced argument also applies, namely "the prior art only teaches a single configurable state while applicants' specification (and the claimed subject matter) clearly recites that the apparatus can be configurable as both" (Reply Br. 3). On this record, we are unable to reasonably ascertain that Voth teaches or suggests use of a processor or some other circuit to arrange node equipment to operate as masters or slaves.

In conclusion, the Examiner at most has merely provided Yamanaka and Voth column, line number and figure citations teaching arrangements for master and slave equipment (Ans. 5, 37). The Examiner, however, has not provided reasoning and rationale for finding the prior art as teaching or suggesting configuring components as both master and slave equipment as claim 1 requires, or that the "synchronization circuit is configurable *by the host*" (as one of a master and slave) as claims 39 and 52 require (emphasis added). For us to affirm on this record would require speculation as to bases for the Examiner's findings.

For the foregoing reasons, Appellants have persuaded us of error in the Examiner's rejection of representative claim 1. Therefore, we will not sustain the Examiner's rejection of that claim, claims 3-7, 13-28, 30-34, 38-46, and 48-53 for similar reasons.

Obviousness over Yamanaka, Voth, and Rasmussen

Claims 8-12

Appellants' sole argument is that claims 8-12 depends from claim 1, and that Rasmussen fails to cure Yamanaka and Voth prior asserted deficiencies in teaching or suggesting configurability of both master and slaves for synchronization (App. Br. 12, 13). The Examiner indicates that Appellants' argument fails because Yamanaka and Voth are not deficient as asserted by Appellants (Ans. 38).

We find that Rasmussen teaches a computerized control system that uses synchronized multiple processor control units (FF 5), but we are unable to reasonably ascertain that Rasmussen alone or in combination with Yamanaka and/or Voth teaches or suggests the claim 1 disputed limitation. Therefore, we conclude that Rasmussen does not cure Yamanaka and Voth deficiencies noted above with respect to claim 1. We, accordingly, will not sustain the obviousness rejection of claims 8-12 for similar reasons.

Obviousness over Yamanaka, Voth, and Kuribayashi

Claims 29, 35-37, and 47

Appellants argue *inter alia* that claims 29 and 35-37 depend from claim 1, whereas claim 47 depends from independent claim 39, and Kuribayashi fails to cure Yamanaka and Voth prior asserted deficiencies in teaching or suggesting configurability of both master and slaves for synchronization as recited claims 1 and 39 (App. Br. 13). We do not find that the Examiner addresses this argument.

We find that Kuribayashi teaches a communication control apparatus that sets synchronization for a master and slave through referencing stored information (FF 6), but we are unable to reasonably ascertain that

Kuribayashi alone or in combination with Yamanaka and/or Voth teaches or suggests the disputed limitations of claims 1 and 39. Therefore, we conclude that Kuribayashi does not cure Yamanaka and Voth deficiencies noted above. We, accordingly, will not sustain the obviousness rejection of claims 29, 35-37, and 47 for similar reasons.

CONCLUSION

Appellants have shown that the Examiner erred in rejecting claims 1 and 3-53 under § 103.

ORDER

The Examiner's decision rejecting claims 1 and 3-53 is reversed.

REVERSED

KIS

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